SPECIFICATION

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CLOCK SIGNAL DISTRIBUTION UTILIZING DIFFERENTIAL SINUSOIDAL SIGNAL PAIR

Background of the Invention

[0001] FIELD OF THE INVENTION

[0002] This invention is concerned with integrated circuits (ICs), and is more particularly concerned with distribution of clock signals on an IC.

[0003] BACKGROUND OF THE INVENTION

[0004] At the current state of the art, processors are operating at clock rates of 1 GHz or higher, and further advances in operating rates can be anticipated. However, at current and expected future clock rates, noise generation and power consumption are significant issues in connection with clock signal distribution. For example, in one processor operating at 1 GHz, the power consumption of the clock tree accounts for about 75% of the power consumed by the chip.

[0005] Furthermore, with conventional clock distribution techniques it has been considered desirable to limit the amount of clock gating employed in processors operating at the high frequencies referred to above, since turning on and off gated clocks may result in noise spikes.

[0006] Accordingly, it would be desirable to provide clock signal distribution in a manner that accommodates very high clock frequencies with a reduced noise profile and reduced power consumption.

Brief Summary of the Invention

[0007] SUMMARY OF THE INVENTION

[0008] According to an aspect of the invention, a method of generating a clock signal on an IC is

provided. The method includes generating a differential sinusoidal signal pair, and generating a clock signal from the differential sinusoidal signal pair for the IC.

[0009] According to another aspect of the invention a method of driving a clock tree on an IC includes distributing a clock signal in the form of a differential sinusoidal signal pair in a portion of the clock tree.

[0010] According to still another aspect of the invention, a clock circuit for an IC includes a generating circuit for generating a differential sinusoidal signal pair, a distribution circuit coupled to the generating circuit for distributing the differential sinusoidal signal pair on the IC, and a plurality of clock receiver circuits coupled to the distribution circuit for converting the differential sinusoidal signal pair into respective local clock signals.

[0011] Since a differential sinusoidal signal pair is used for distributing the clock signal, very low-swing signals may be employed, thereby greatly economizing on power consumption. Moreover, since local clock signal regeneration is performed on a differential basis with reference to the distributed pair of signals, noise which couples to both of the pair of signals is automatically filtered out. Also, since the clock signal is sinusoidal prior to regenerating, its energy is concentrated at the clock frequency rather than being spread through the spectrum as in the case of a square wave clock signal. Consequently, energy efficiency is promoted.

[0012] Other objects, features and advantages of the present invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

Brief Description of the Several Views of the Drawings

[0013] BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 is a schematic block diagram representation of a clock signal generation and distribution arrangement provided in accordance with the invention; and

[0015] FIG. 2 is a schematic diagram of a typical one of the clock receivers shown in FIG. 1.

Detailed Description of the Invention

[0016] DETAILED DESCRIPTION

[0017] FIG. 1 is a schematic block diagram representation of a clock signal generation and distribution arrangement provided in accordance with the invention.

[0018] In FIG. 1, reference numeral 10 indicates a signal generator which generates a differential sinusoidal signal pair. As is well understood by those who are skilled in the art, a differential sinusoidal signal pair comprises a pair of sinusoidal wave forms, that are substantially equal in frequency and amplitude but that are substantially 180Â° out of phase with each other. The differential sinusoidal signal pair generated by signal generator 10 may, for example, have a peak to peak differential (ppD) of about 100 mV or 150 mV. The common mode level of the differential sinusoidal signal pair may be at the center of the power supply voltage. For example, each signal of the pair may swing from about 575 mV to 625 mV when a 1.2 volt power supply is used. It will be recognized that such a differential sinusoidal signal pair has a peak to peak differential of 100 mV. It is contemplated to employ a differential sinusoidal pair having a different common mode and/or a different peak to peak differential than the signals which have been described above.

[0019] It is well within the ability of those who are skilled in the art to design a suitable signal generator to generate the differential sinusoidal signal pair as described above using conventional circuit design techniques. Accordingly, it is not necessary to describe the design of the signal generator 10.

[0020] Continuing to refer to FIG. 1, distribution circuitry 12 is coupled to signal generator 10. The distribution circuitry 12 distributes the differential sinusoidal signal pair from the signal generator 10 to points on an integrated circuit at which local clock signals are to be generated (as described below).

[0021] In order to provide for minimal skew, in at least one embodiment of the invention it is preferred that the distribution circuitry 12 include adjacent tracks of metal lines through which the respective signals of the differential sinusoidal signal pair are routed together (e.g., so that each signal travels approximately the same distance). It is also preferred that there be one or two tracks of isolation between the respective tracks for the signal pair to reduce mutual coupling capacitance. Such a routing layout can be provided using commercially available routing tools. Other routing layouts may be employed.

[0022] Because it is contemplated to use very small swing signals for the differential sinusoidal

signal pair, the additional capacitance resulting from two clock signal nets instead of one is more than compensated for relative to the capacitance that would be generated by a single full-swing digital clock.

[0023] It may be desirable for that the distribution circuitry 12 to be routed and loaded so as to have inductance and capacitance that produces resonance at the desired frequency of operation. This further reduces the clock power requirements. Switchable loads 14 may be included in the distribution circuitry 12 to permit the load of the distribution circuitry 12 to be tuned to compensate for manufacturing variations.

[0024] Coupled to the distribution circuitry 12 are clock receivers 16. The purpose of the clock receivers 16 is to receive the differential sinusoidal signal pair distributed through the distribution circuitry 12 and to convert the differential sinusoidal signal pair to local clock signals having a suitable wave form and amplitude. The local clock signals may, but need not be, in the form of a square wave. The local clock signals output by the clock receivers 16 may, for example, swing from substantially zero volts to substantially the level of the power supply, which may be 1.2 volts or any other suitable voltage. It will accordingly be recognized that the peak to peak differential of the differential sinusoidal signal pair distributed through the distribution circuitry 12 may be on the order of less than half or less than one-fifth or even less than one-tenth of the amplitude of the local clock signals outputted from the clock receivers 16.

[0025] The number of clock receivers 16 may vary, and depends on the architecture of the IC for which clock distribution is to be provided.

[0026] The clock receivers 16 may comprise, for example, differential amplifiers such as the differential-to-single-ended converter illustrated in FIG. 2. The circuit shown in FIG. 2 is similar to conventional differential-to-single-ended converters and accordingly need not be described in detail. It will be observed that the circuit of FIG. 2 includes a first differential amplification stage 18 and a second differential amplification stage 20. The first differential amplification stage 18 and the second differential amplification stage 20 are respectively dc biased by FETs 22 and 24 and are coupled with opposite polarity to the differential sinusoidal signal pair supplied at inputs 26 and 28. FET 30 is provided so that a predictable current is supplied to FETs 22 and 24 (e.g., from a current source provided via input IREF).

[0027] Downstream from the amplification stages 18 and 20 are a third amplification stage 32 and output stages 34.

[0028] In the embodiment of FIG. 2, the first and second amplification stages 18, 20 each an NMOS differential transistor pair 18a, 20a with PMOS current mirror active loads 186, 206. The third amplification stage 32 comprises a PMOS differential pair (forward from transistors 32a, 32b) with an NMOS current mirror active load 32c. The output stages 34 comprise three conventional series-connected FET inverters 34a, 34b and 34c which produce complimentary outputs 35a, 35b. Other differential transistor pair configurations and/or buffering output stages may be employed.

[0029] In operation, the differential sinusoidal signal pair is provided to the inputs 26, 28. In response thereto, the first amplification stage 18 produces a first input to the third amplification stage 32 that is proportional to the difference between the inputs 26, 28. Similarly, the second amplification stage 20 produces a second input to the third amplification stage 32 that is proportional to the difference between the inputs 26, 28, but that is of opposite polarity to the first input provided by the first amplification stage 18. The third amplification stage 32 comprises the difference between the first and second inputs thereto (e.g., about twice the value of the output of either the first or second amplification stages 18, 20) to produce an output that is fed to the output stages 34. The output stages 34 further amplify the output of the third amplification stage 32 to produce complimentary outputs 35a, 35b that fully transition between ground (e.g. V_{SS}) and the power supply rail (e.g., V_{DD}).

[0030] Because the inputs 26, 28 to the clock receiver circuit 16 shown in FIG. 2 are routed together, any noise experienced by one of the inputs is also experienced by the other input, and such noise is filtered by the clock receiver circuit 16 because it is a differential amplifier. Because of the noise immunity provided by the clock receiver circuits 16, the signals distributed to the distribution circuit 12 may have very low voltage swings, which results in reduced power dissipation.

[0031] If the clock receiver circuit 16 shown in FIG. 2 is balanced, then the output signals have 50% duty cycle. Ideally, the outputs 35a, 35b are non-overlapping (e.g., the output 35a is never high at the same time that the output 35b is high, or vice versa, as the outputs 35a, 35b are complimentary. It is also contemplated to create imbalances in the clock receiver circuit 16 of FIG. 2 by, e.g., arranging the dimensions of pairs of FETs to be different within one or more of

the amplification stages 18, 20, 32 to create a non-50% duty cycle. In general, any technique that can controllably introduce asymmetry to differential amplifier transistor pairs may be similarly employed (e.g., manipulating doping levels, threshold voltage implant doses, etc.). In this way, the purely differential input could be converted to a set of non-overlapping clock signals, which would be suitable for use with latches that call for non-overlapping clocks.

[0032] Those who are skilled in the art will recognize that many modifications and variations of the circuit shown in FIG. 2 would be suitable for use as the clock receivers 16 of FIG. 1. Design of this or other suitable types of clock receiver circuitry is well within the ability of those who are skilled in the art.

[0033] Referring once more to FIG. 1, clock splitters 36 are provided downstream from clock receivers 16. In one embodiment of the invention, about ten clock splitters 36 are coupled to each clock receiver 16. Other numbers of clock splitters may be coupled to each clock receiver 16. The clock splitters 36 are provided for further distribution of the regenerated clock signals output from the clock receivers 16 (as is known in the art). The clock splitters 36 also generate non-overlapping clocks for latches which call for such signals. Any conventional clock splitters may be employed for the clock splitters 36.

[0034] Because of the low noise profile of the clock distribution system illustrated in FIG. 1, it is feasible to employ a substantial amount of clock gating. The clock gating may be implemented, for example, by selectively gating off the clock receivers 16 using any conventional clock gating technique.

[0035] From the foregoing description it will be understood that all of the signal generator 10, the distribution circuitry 12, the clock receivers 16 and the clock splitters 36 may be formed on an integrated circuit (IC) 38 such as a microprocessor. It will also be recognized that the circuitry between signal generator 10 and the outputs of clock splitters 36 constitutes some or all of a clock tree.

[0036] With the clock signal distribution arrangement provided in accordance with the present invention, power consumption is reduced and noise generation is minimized, as compared to conventional clock signal distribution techniques. The present invention also accommodates clock gating and generation of a set of non-overlapping clocks.

[0037] The foregoing description discloses only the exemplary embodiments of the invention;

modifications of the above disclosed apparatus and methods which fall within the scope of the invention will be readily apparent to those of ordinary skill in the art. For example, although the present invention is particularly suited for application to microprocessors, it may also be used in connection with any other type of integrated circuit for which clock distribution is employed.

[0038] While the present invention has been disclosed in connection with exemplary embodiments thereof, it should be understood that other embodiments may fall within the spirit and scope of the invention, as defined by the following claims.